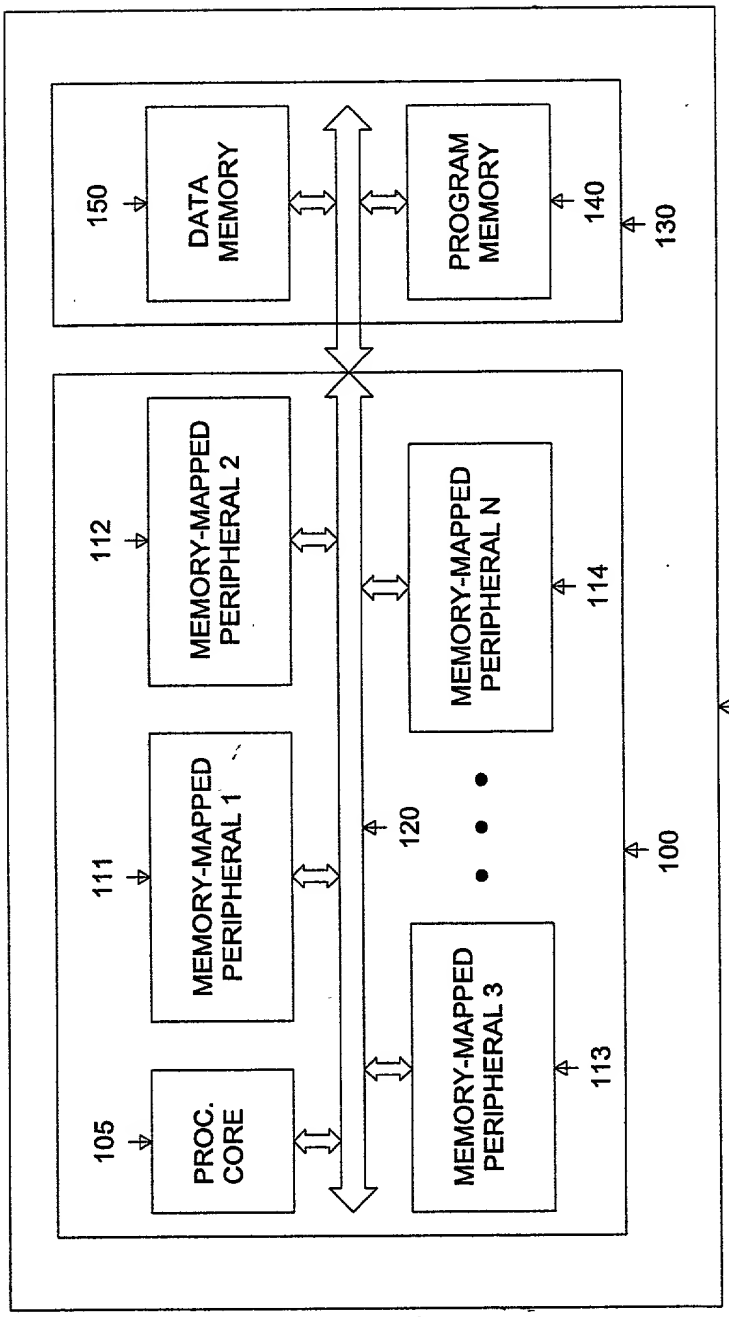
10
100
105
PROC. CORE
111
MEMORY-MAPPED PERIPHERAL 1
112
MEMORY-MAPPED PERIPHERAL 2
113
MEMORY-MAPPED PERIPHERAL 3
114
MEMORY-MAPPED PERIPHERAL N
120
130
140
PROGRAM MEMORY
150
DATA MEMORY

FIGURE 1

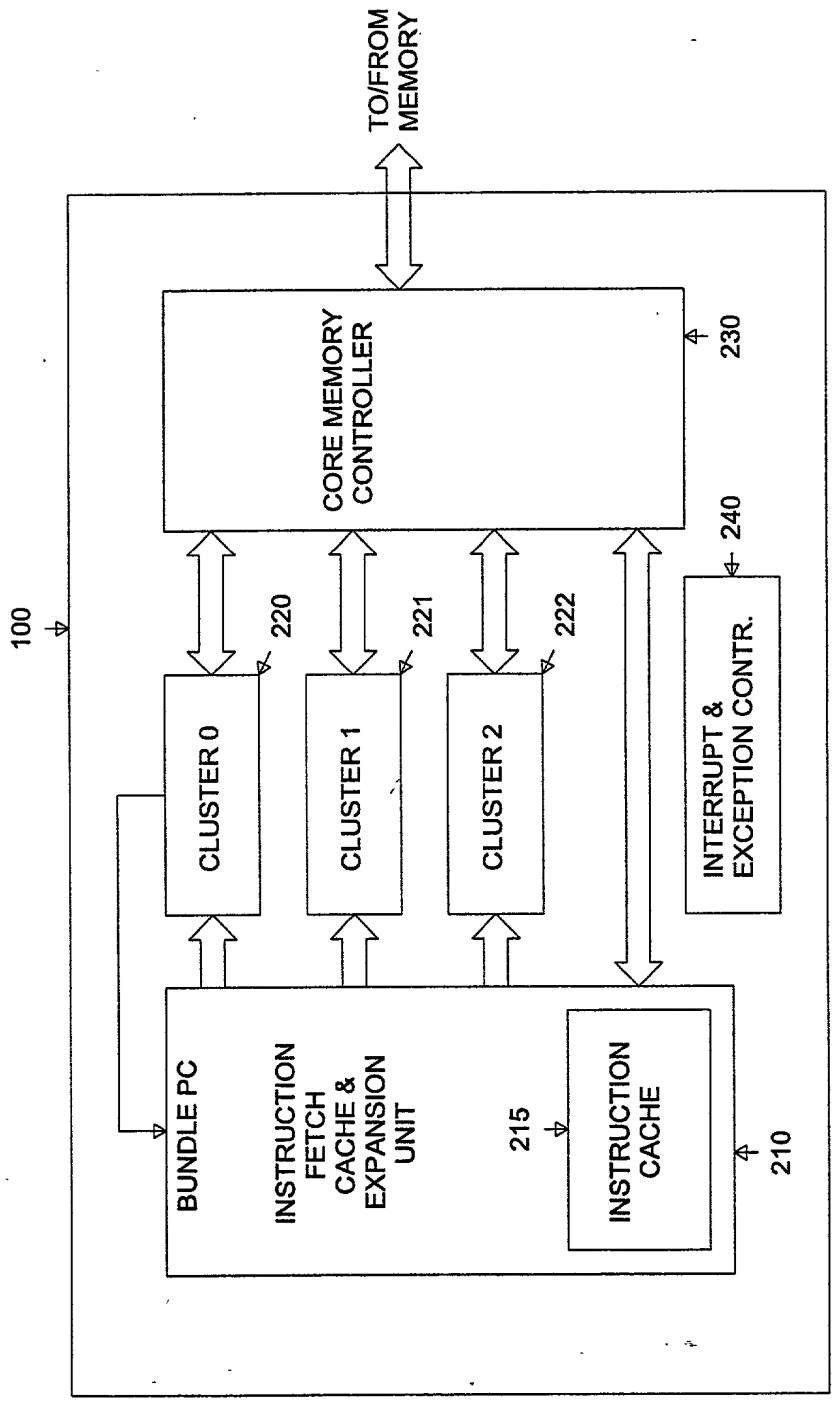
TO/FROM MEMORY
CORE MEMORY CONTROLLER
230
240
100
220
221
222
CLUSTER 0
CLUSTER 1
CLUSTER 2
INTERRUPT & EXCEPTION CONTR.
BUNDLE PC
INSTRUCTION FETCH CACHE & EXPANSION UNIT
215
INSTRUCTION CACHE
210

FIGURE 2

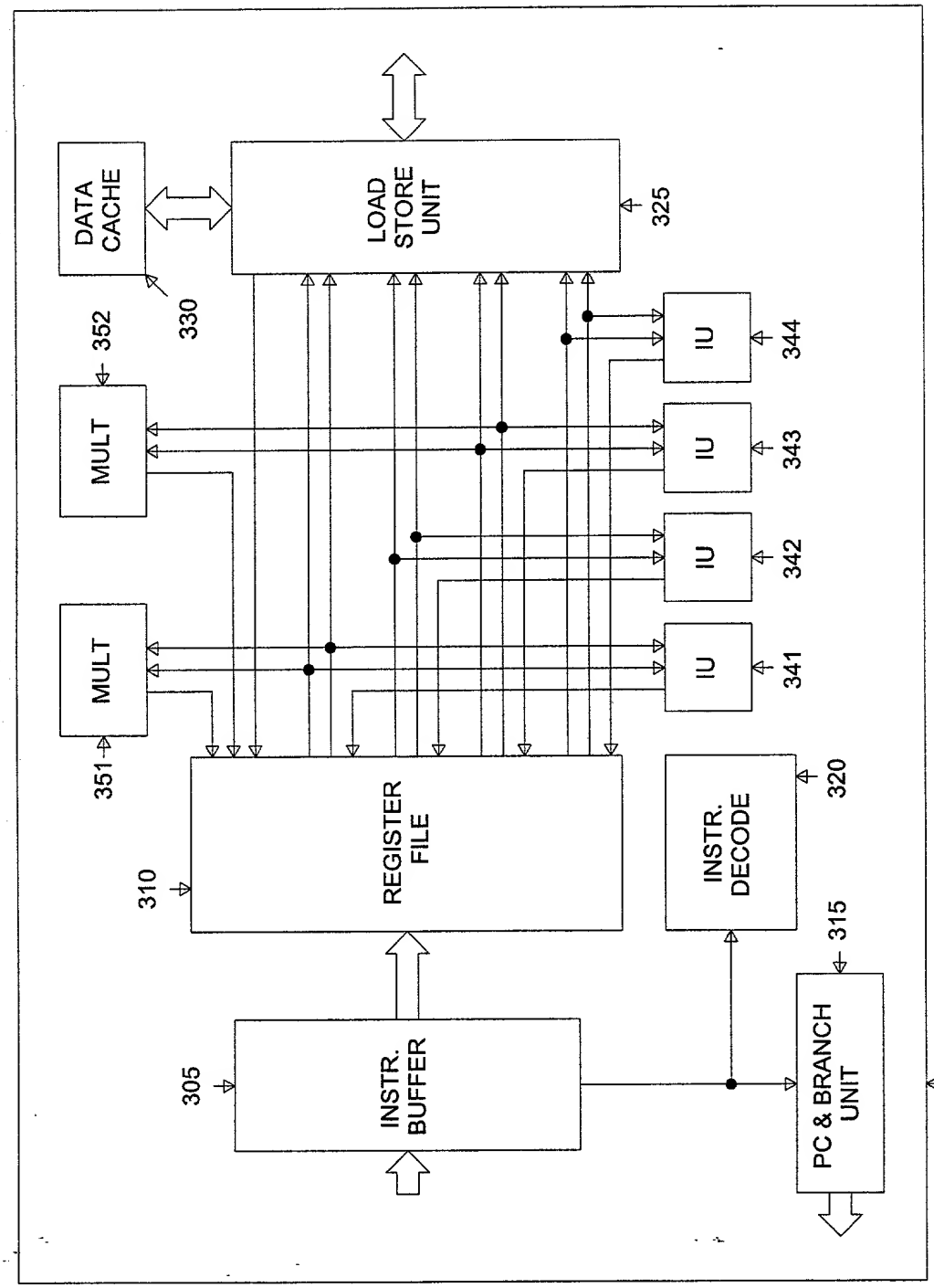
DATA CACHE
330
LOAD STORE UNIT
325
352
MULT
351
MULT
IU
344
IU
343
IU
342
IU
341
310
REGISTER FILE
INSTR. DECODE
320
315
305
INSTR. BUFFER
PC & BRANCH UNIT
220

FIGURE 3

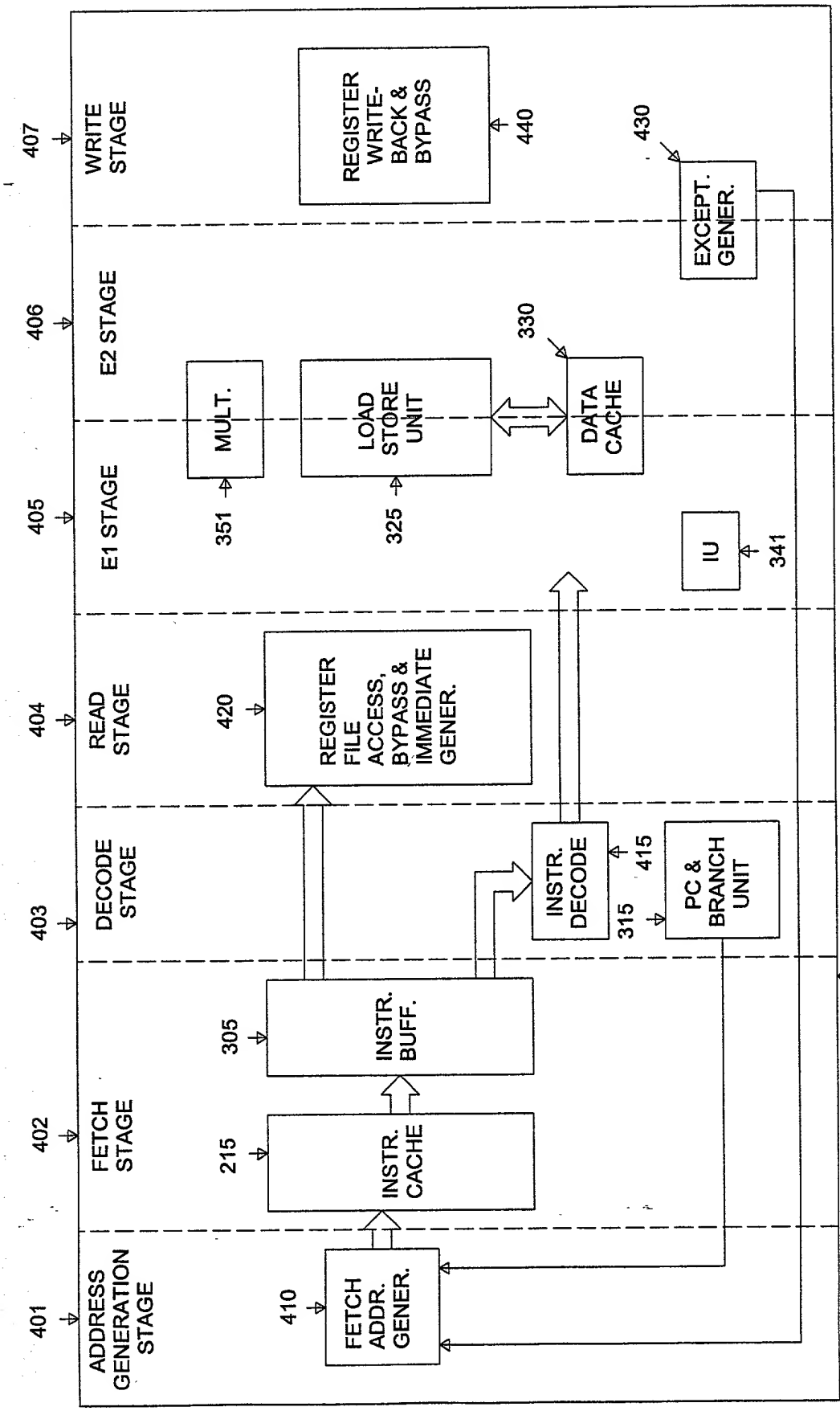
ADDRESS GENERATION STAGE
401
FETCH ADDR. GENER.
410
FETCH STAGE
402
INSTR. CACHE
215
INSTR. BUFF.
305
DECODE STAGE
403
INSTR. DECODE
315
PC & BRANCH UNIT
415
READ STAGE
404
REGISTER FILE ACCESS, BYPASS & IMMEDIATE GENER.
420
E1 STAGE
405
MULT.
351
LOAD STORE UNIT
325
IU
341
E2 STAGE
406
DATA CACHE
330
WRITE STAGE
407
REGISTER WRITE-BACK & BYPASS
440
EXCEPT. GENER.
430
100
400

FIGURE 4

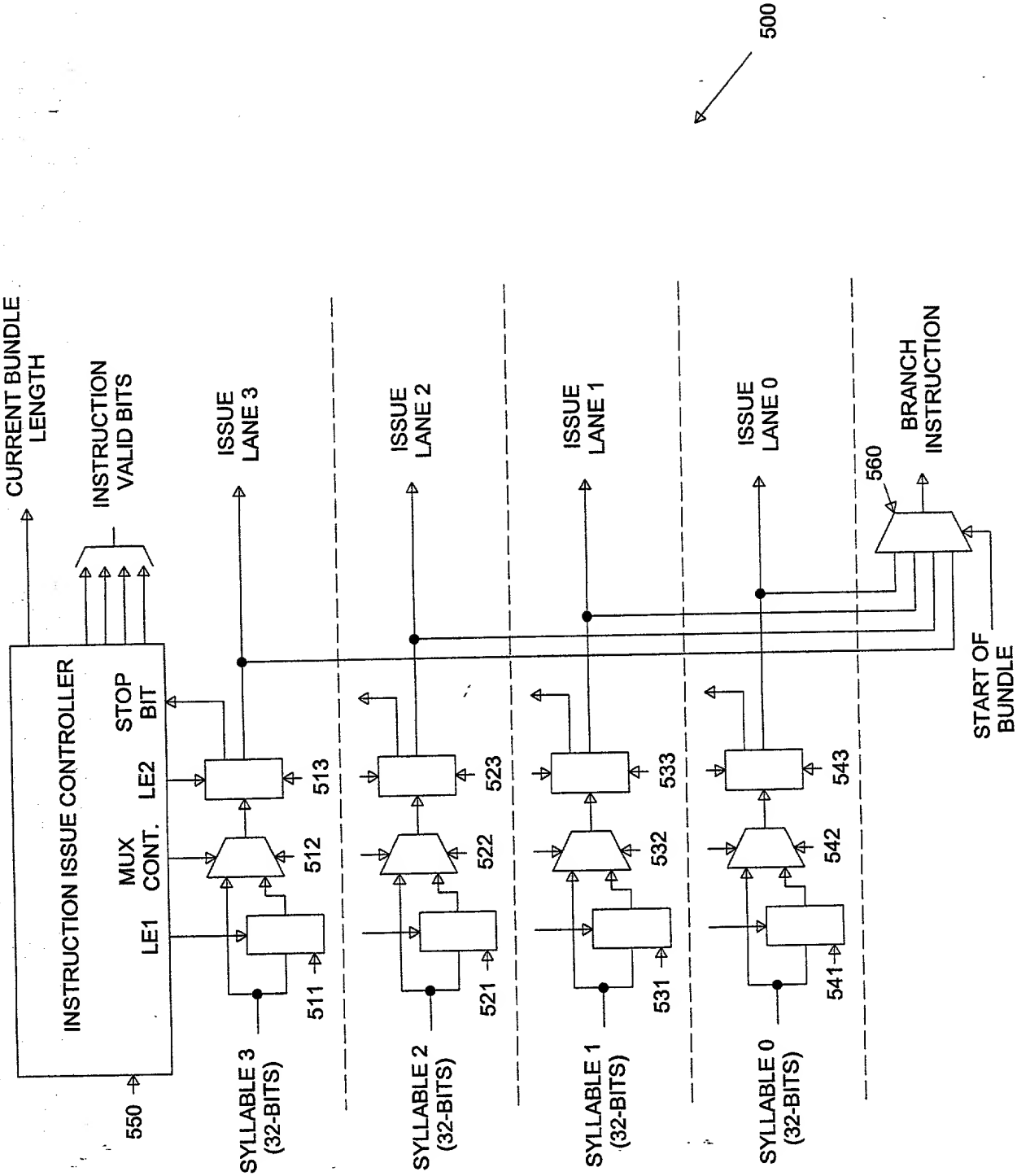
500
CURRENT BUNDLE LENGTH
INSTRUCTION VALID BITS
ISSUE LANE 3
ISSUE LANE 2
ISSUE LANE 1
ISSUE LANE 0
BRANCH INSTRUCTION
560
INSTRUCTION ISSUE CONTROLLER
STOP BIT
LE2
MUX CONT.
LE1
550
513
512
511
523
522
521
533
532
531
543
542
541
SYLLABLE 3 (32-BITS)
SYLLABLE 2 (32-BITS)
SYLLABLE 1 (32-BITS)
SYLLABLE 0 (32-BITS)
START OF BUNDLE

FIGURE 5

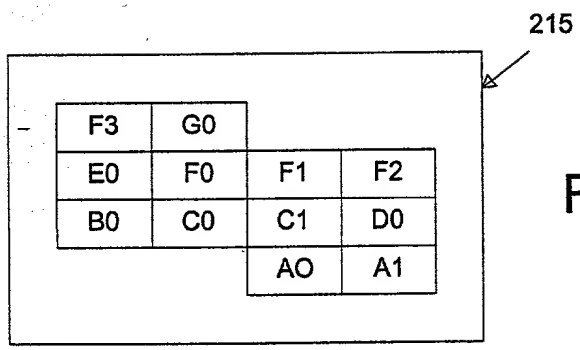

FIGURE 6

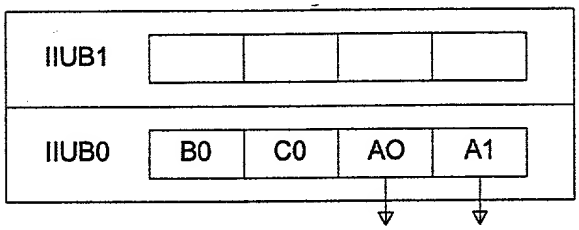

FIGURE 7A

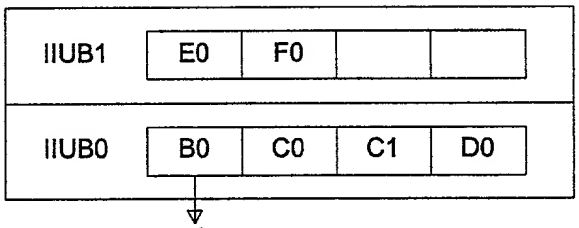

FIGURE 7B

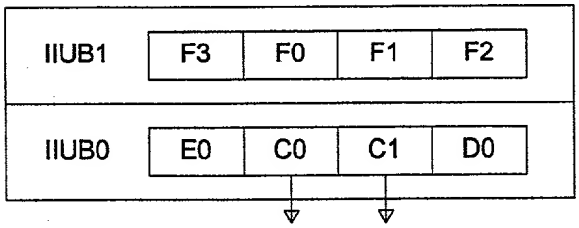

FIGURE 7C

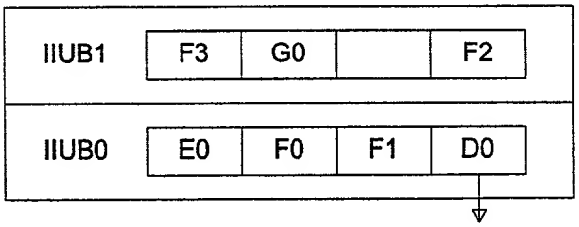

FIGURE 7D

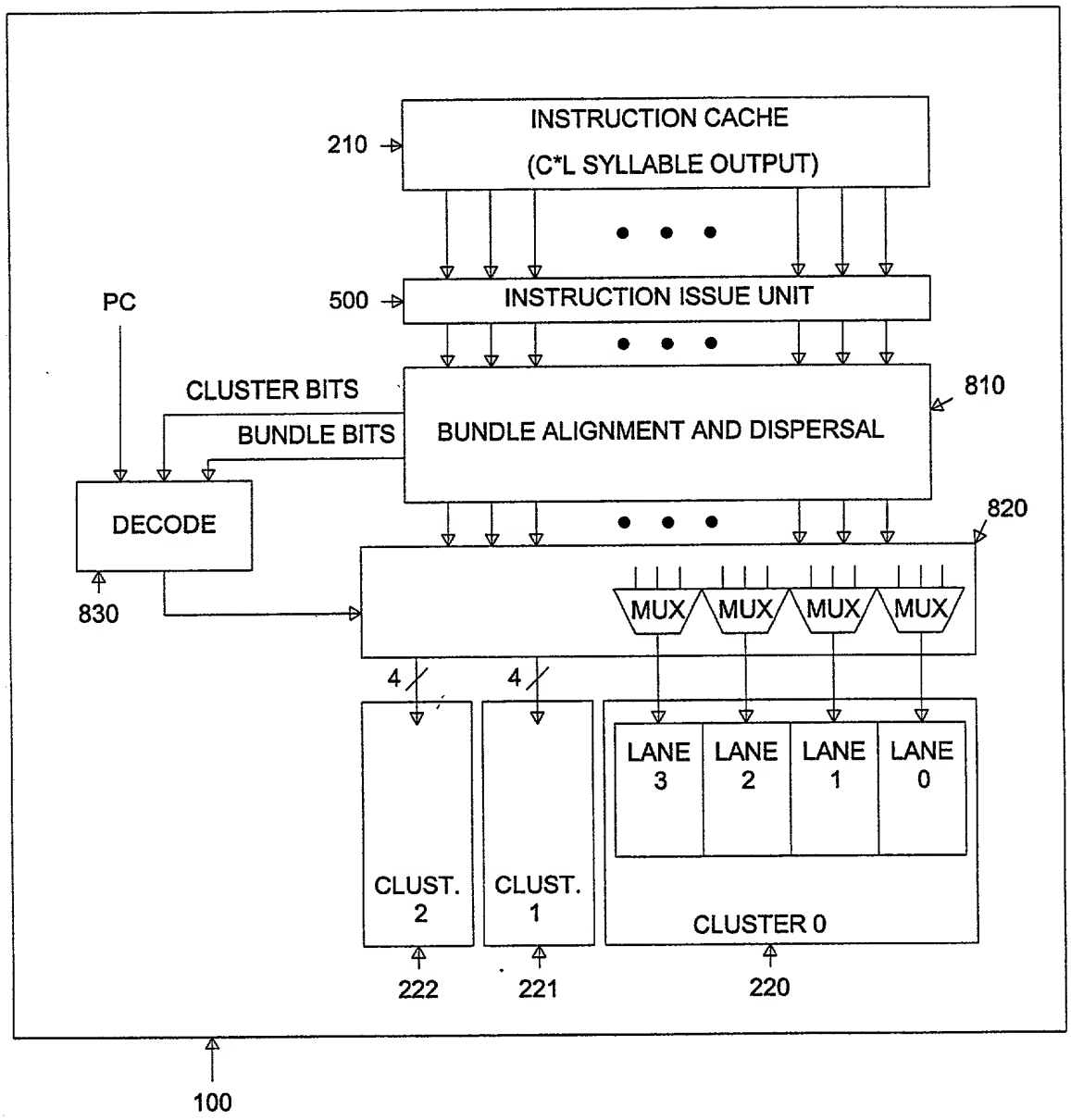
INSTRUCTION CACHE
(C*L SYLLABLE OUTPUT)
210
INSTRUCTION ISSUE UNIT
500
PC
CLUSTER BITS
BUNDLE BITS
BUNDLE ALIGNMENT AND DISPERSAL
810
DECODE
820
830
MUX
MUX
MUX
MUX
4
4
LANE 3
LANE 2
LANE 1
LANE 0
CLUST. 2
CLUST. 1
CLUSTER 0
222
221
220
100

FIGURE 8